The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-14. (Canceled)

15. (New) An information processing apparatus comprising a plurality of hardware circuit blocks, each configured so as to implement one of functional units of certain information processing software as hardware, the plurality of hardware circuit blocks mutually operating in pipeline, each of the plurality of hardware circuit blocks comprising:

a first processing circuit module connected to a memory for operating to selectively make read access or write access to the memory in response to the input of packet data and on the basis of the content of the packet;

a second processing circuit module for operating to receive packet data outputted from the first processing module to create packet data obtained by subjecting a predetermined information process to the received packet; and

an interface module for operating to receive input packet data to each hardware circuit block and the packet data created by the second processing circuit module to provide these received packet data to the first processing circuit module at separate timing,

wherein the first processing circuit module responds to either one of the input packet data provided via the interface circuit module and the packet data subjected to the predetermined information process so that when responding to the input packet data the first processing circuit module reads out of the memory information data needed to process the input packet data and when responding to the packet data subjected to the predetermined information process the first processing circuit module writes new

information data associated with that packet data into the memory while causing each hardware circuit block to output the packet data subjected to the predetermined information process.

16. (New) An information processing apparatus comprising a plurality of hardware circuit blocks each of which functions to output packet data by subjecting a specific information process to given input packet data, the plurality of hardware circuit blocks mutually operating in pipeline, each of the hardware circuit blocks comprising:

a first processing circuit module connected to a memory for operating to selectively read or write information data from or into the memory, the first processing circuit module receiving the input packet data to read out information data needed for processing from the memory on the basis of the content of the received packet data and to output packet data obtained by adding the needed information data to the input packet data;

a second processing module for receiving the packet data with the needed information data being added outputted from the first processing circuit module to create packet data obtained by subjecting a predetermined information process to the received packet data while creating new information data; and

a merging circuit module having a plurality of input terminals, to which a plurality of pieces of packet data are inputted in parallel, for outputting the plurality of pieces of packet data in serial in an inputted order without subjecting any process to the inputted packet data,

wherein the information processing apparatus is configured in such a way that the input packet data is inputted from one input terminal of the merging circuit module and the output of the second processing circuit module is connected to another of the merging circuit module and that the output data from the second processing circuit module is inputted via the merging circuit module to the first processing circuit module and then new information data extracted from the output data inputted to the first

processing circuit module is written into the memory while outputting the packet data subjected to the information process from the hardware circuit block.

17. (New) An information processing apparatus comprising a plurality of hardware circuit blocks each of which is adapted to subject a specific information process to given input packet data to output processed packet data, the plurality of hardware circuit blocks mutually operating in pipeline, each of the plurality of hardware circuit modules comprising:

a first processing circuit module which operates to receive packet data and to selectively make read access or write access to a memory;

a second processing circuit module for receiving packet data and information data needed to process the packet data to create packet data obtained by subjecting a predetermined information process to the packet data and to create new information data needed to process the packet data; and

a merging circuit module having a plurality of parallel input terminals and a single output terminal for outputting a plurality of pieces of inputted packet from the single output terminal in inputted order without subjecting any information process to the inputted packet data,

wherein the first processing circuit module selectively operates on the basis of the packet data outputted from the merging circuit module in either one of (i) a read mode in which the memory is accessed to read information data needed to process the input packet data, and (ii) a write mode in which the packet data subjected to the predetermined information process created by the second processing circuit module and the new information data to write the new information data into the memory while outputting the packet data subjected to the information process from each hardware circuit block.

18. (New) An information processing apparatus having a plurality of hardware circuit blocks constructed from software which is adapted to process input packet data on the basis of information data stored in a memory to output the processed packet data, the software comprising (i) a first function in which the input packet data is received, information data needed to process the received packet data is read out of the memory and the input packet data is returned together with the information data, (ii) a second function in which a predetermined information process is subjected to the input packet data on the basis of a result of the process by the first function while creating new information data, and (iii) the information data stored in the memory rewritten on the basis of a result of the process by the second function and the content to packet data be outputted is returned, each of the plurality of hardware circuit blocks comprising:

a first hardware module capable of selectively executing either the process by the first function or the process by the third function in response to the input packet data and on the basis of the content thereof;

a second hardware module capable of executing the process by the second function; and

an interface for receiving in parallel the input packet data and the packet data outputted from the second hardware module and for sequentially outputting these packet data to transfer the outputted packet data to the first hardware module.

19. (New) The information processing apparatus according to any one of claims 15 to 18, wherein the hardware circuit blocks comprise a plurality of hardware circuit blocks disposed in parallel, which fulfill the same element functions so as to resolve bottlenecking in the processing speed of the apparatus.

20. (New) The information processing apparatus according to any one of claims 15 to 18, wherein a portion of the information processing is performed by software

program on a general-purpose computer and an input/output from the computer is connected to the processing circuit modules and/or the merging circuit module.

21. (New) The information processing apparatus according to any one of claims 15 to 18, wherein the predetermined process comprises an internet server process.

22. (New) The information processing apparatus according to any one of claims 15 to 18, wherein the hardware circuit block is directly connected the another hardware circuit block or connected via the merging circuit module.

23. (New) A method for processing information in a hardware circuit block comprising a first processing circuit module adapted to access a memory to selectively read or write information data from or into the memory and a second processing circuit module adapted to subject a specified information process to given packet data using the information data stored in the memory, the hardware circuit block operating in pipeline in conjunction with another hardware circuit block, the method comprising the steps of:

receiving module by the first processing circuit input packet data and reading information data needed to process the input packet data out of the memory on the basis of the content of the input packet data to output the read information data together with the input packet data;

receiving by the second processing circuit module the input packet data and information data outputted from the first processing module and subjecting a predetermined process to the input packet data using the information data while newly creating information data needed to process another packet data; and

receiving by the first processing circuit module the packet data subjected to the predetermined process and the newly created information data and writing the newly

created information data into the memory while outputting the packet data subjected to the predetermined process to the outside of the hardware circuit block.